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WAFER LEVEL PACKAGE FOR PRODUCING CHIP SIZE PACKAGES AND METHOD OF FABRICATING THE SAME

Field of the invention

The present invention relates to a semiconductor package, and more specifically, to a wafer level packaging technology and a method for forming the wafer level package.

Background

In recent progress of integrated circuit devices, since the chips are manufactured toward a trend of high density, it also has a trend to make semiconductor devices have smaller size in order to contain more IC in the devices. IC designers are attempted to scale down the size of devices and increase chip integration in a much smaller space. Typically, the semiconductor devices need a protection to prevent the penetration of moisture or the damage caused by accidentally damage. Owing to this, the device structure needs to be packaged by some appropriate technology. In this technology, the semiconductor dies or chips are usually packaged in a plastic or ceramic package. The package of the chips must have the function to protect the chips from being damaged and to release the heat generated by the chips while they are under operation.

The previous packaging technology was mainly based on a concept of a lead frame, using a lead leg as an I/O signal exchange channel. But now, under the highly integrated requirement of the I/O signal exchange, the traditional lead frame

packaging can't totally meet the demand of this requirement. Under this consideration, the packaging needs to be smaller in volume in order to meet the highly integrated requirement. Highly integrated I/O packaging concept also brings the development and a breakthrough in the package technology. A method named as ball grid array (BGA) technology is a popular used method in recent year. Integrated circuit (IC) manufacture companies tend to adapt ball grid array (BGA) technology because the lead leg used by BGA is a ball-shaped leg instead of the slender leg used by the traditional lead frame technology. Another advantage of BGA also includes that the pitches (distance between balls) are smaller and are not easily deformed because of their ball-shaped legs. The smaller distances between balls reveal that the signal transportation would also become quicker than the traditional lead frame technology The U. S. patent No. 5629835, proposed by Mahulikar, et. al, which entitled" METAL BALL GRID ARRAY PACKAGE WITH IMPROVED THERMAL CONDUCTIVITY" states a ball grid array packaging method. Another U.S. patent No.5239198 discloses a packaging form, which consists a substrate using FR4 material to form a screen printing package.

Various integrated circuit packagings have been developed in recent years, however no matter what kind it is. Most of them adapt the following procedures in dividing the wafer: First, cutting the wafer into individual chips, then proceeding the packaging and testing steps. However, in U.S. patent No. 5323051 "SEMICONDUCTOR WAFER LEVEL PACKAGING", it reveals a packaging step. The packaging step is conducted before cutting the wafers. It uses glass as adhesive material to seal the device in a hole. A covered hole is allowed to be the electric channel. The wafer level packaging is another manufacture trend for semiconductor package. One of the previous inventions is to form a plurality of dies on a surface of a

semiconductor wafer. A glass is attached on a surface of the wafer having dies formed thereon by adhesive material. Then the other surface of the wafer (the surface without dies) is grinded to reduce the thickness of the wafer. This method is called back grinding. Then, the wafer is etched to separate ICs and expose a portion of the adhesive material. Another glass is further attached to the wafer surface with dies by adhesive material. The next step is to form a thin film on the first glass, then etching the first glass and a portion of the adhesive material. This step is called the notch process. Thus forming a trench in the glass and adhesive material. In the next step, Tin ball will be formed on the thin film in the subsequent process. The thin film made by solder will be patterned onto the surface of the first glass and the surface along the trench to provide an electric connection channel. Solder mask is then formed on the surface of the solder thin film surface and the surface of glass to expose the surface for which it is associated with the thin film. Tin ball is formed on the exposed solder thin film by the traditional method. In the next step, the cutting procedure is conducted by etching the adhesive material in the trench to cut through the glass in order to separate the dies. The method mentioned above is complicated, it needs the notch process and cutting the second glass to separate the dies. Besides, the cutting place would become a trench cliff, which is sharp for solder to attach on the cutting place and finally reduce the quality of the device in the package process.

According to the reasons mentioned above, there is a need to provide a more simpler and compact method to the wafer level packaging.

Summary

It is an objective of the invention to provide a chip size packaging.

It is another objective of the invention to provide a wafer level package

method.

It is yet another objective of the invention to provide a wafer level package method suitable for the wafer level packaging test.

The wafer level package comprises a plurality of dies formed on the wafer, I/O metal pads formed on a first surface of the wafer.

Then, coating a photosensitive polymer, for example, photosensitive polyimide film on the first surface, then a portion of the film is removed by laser.

In the next step, coating a first photoresist on a second surface of the wafer. The first photoresist comprises positive photoresist.

Forming a first conductive layer in the hole (opening) of the photosensitive polyimide film and then covering a metal pad. The first conductive layer comprises alloy with the composition of Zn/Ni/Cu.

In the next step, forming a seeding layer with copper on the top of the first conductive layer and the photo sensitive polymer layer. Then, forming a second photoresist on the seeding layer to define the circuit pattern diagram. Then, forming a second conductive layer to the circuit pattern diagram located on the defined area of the second photoresist. The second conductive layer comprises copper.

Removing the second and the first photoresist and the seeding layer covered by the second photoresist, thus forming trenches between each of the packaging entity.

Then, a filling material was filled into the trenches and covers the circuit pattern diagram. The filling material comprises epoxy.

Then, executing a grinding process to grind the second surface of the wafer to expose the filling material. Next, executing an opening step to expose a portion of the circuit pattern diagram to define an area on which a conductive convex block to

be formed.

Executing a solder screen printing step to form a solder paste area, then reflowing this area to form the conductive convex block.

Brief Description of the Drawing

The foregoing aspects and many of the attendant advantages of this invention will become more readily appreciated as the same becomes better understood by reference to the following detailed description, when taken in conjunction with the accompanying drawings, wherein:

FIG.1 indicates the cross-sectional diagram of a wafer with metal pads formed thereon.

FIG.2 indicates the cross-sectional diagram of a wafer with an opening opened thereon.

FIG.3 indicates the cross-sectional diagram of a wafer with a positive photoresist formed on the back-side of the wafer.

FIG.4 indicates the cross-sectional diagram of a wafer with an electroplating pad wetting layer formed thereon.

FIG.5 indicates the cross-sectional diagram of a wafer with an electroless electroplating copper seeding layer formed thereon.

FIG.6 indicates the cross-sectional diagram of a wafer with coating a photoresist pattern thereon to define a circuit diagram.

FIG.7 indicates the cross-sectional diagram of a wafer with a copper layer formed by electroplating.

FIG.8 indicates the cross-sectional diagram of a wafer with the situation of photoresist removed.

FIG.9 indicates the cross-sectional diagram of a wafer with trenches having a filling material filled formed therein.

FIG.10 indicates the cross-sectional diagram of a wafer with back-side grinding surface.

FIG.11 indicates the cross-sectional diagram of a wafer with Tin balls formed therein.

FIG.12 indicates the cross-sectional diagram of a wafer after the wafer level package testing.

FIG.13. indicates the cross-sectional diagram of a wafer after cutting (dividing) of the wafer level package.

Detailed Description of the preferred embodiments

This invention discloses a wafer level package and a method for manufacturing the wafer level package. The detail procedure is shown below: First referring to FIG.1 and FIG.2, a surface (the first surface) of a wafer 2 has metal pads 4 for input and output signal (I / O pad) and a window 6 is also formed on the surface of the wafer 2 for laser repair. Then, a photosensitive polymer 8 as an insulator layer is formed on the first surface of the wafer 2. The preferred material for photosensitive polymer 8 could be photosensitive polyimide or epoxy. A curing process by ultra violet radiation or heating process is conducted to enhance the structure of epoxy. Then, forming a plurality of openings 9 in the insulator layer 8, each opening is opened associated with the metal pad 4. These metal pads 4 are thus exposed with no coverage. It should be noticed that the photosensitive polyimide or epoxy are transparent material with respect to laser, so the alignment mark on the

scribble line will not be covered by the insulator layer 8. In other words, the label is visible to the alignment tools and can be easily seen in the next operation.

Another way of forming an opening 9 in order to expose the metal pad 4 can also be conducted as follows: Using a mask with some certain pattern to transfer the pattern onto the photoresist, and after the etching process to remove the photosensitive polyimide or epoxy, this can also be done to form the opening 9.

Referring to FIG.3, a photoresist 10 is coated on a second surface of the wafer 2, and a wetting layer 12 is filled into to the opening 9, and the material for wetting layer 12 can be metal or alloy such as Tin/Ni/Cu. Typically, the wetting layer 12 can be formed by electroplating.

Next referring to FIG. 5, a copper seeding layer 14 could be used by electroless Cu plating method to implant the copper seeding layer 14 on the surface of the film 8 and the wetting layer 12. Next, a photoresist pattern 16 is coated on the copper seeding layer 14 to define a metal wire pattern. In FIG.6, using the photoresist pattern 16 as a barrier, a metal (copper) wire 18 is formed on the portion of the area, which is an area not to be covered by the photoresist pattern 16. The formation of the metal wire 18 can be conducted using plating method or other method to form the pattern on the surface of the wafer 2, as shown in FIG.7. Next, removing the photoresist pattern16 and the copper seeding layer 14. During the removing step, although a very thin layer of the metal wire layer 18 may be removed a little bit yet it would do little harm to the whole structure. In this way, the I/O metal pad 4 can be directed through the wetting layer 12 to form an electric connection with the metal layer 18. This process is called re-distribution.

Referring to FIG.9, etching the first surface of the wafer 2, thus forming trenches 20 which can be used in the further manufacture step. A filling material 22

is filled in the trenches 20 to cover the metal wire 18 for insulation and adhesion for the packaging entity. The filling material can be epoxy coated by vacuum coating process. The vacuum coating process can prevent the occurrence of bubbles formed therein. The filling material of epoxy is filled in every packaging entity. In the next step, a curing process such as ultra violet radiation or heating process is conducted to enhance the epoxy structure. A back-side wafer grinding process is conducted in the next step to grind the second surface (the side without circuit lies above) till the bottom of the trench 20 in order to expose the filling material 22, as shown in FIG.10.

Referring to FIG.11, the next step is to define a bump area of solder ball. A portion area of the filling material 22 will be removed and to expose the metal wire 18. The exposed area of the metal wire 18 is aimed to be the site location of the bump. A screen printing method is utilized to coat a layer of solder on the area and to reflow it by thermal process and turning a paste layer of solder into solder ball 24. The solder ball 24 is thus attached to the wafer 2. The formation of solder balls 24 can be conducted by the well-known BGA technology and distributed as an array pattern along the side of a chip. An electric channel is thus constructed by the connection of Tin ball 24 to the metal wire 18. FIG.12 is the diagram showing the wafer level package testing procedure. The wafer 2 is sent to the wafer level testing device for final testing. After the final testing, a cutting (dividing) process is conducted on the wafer 2 to separate the chips. The cutting process is mainly cutted along the trench filled with epoxy, thus producing a chip size package (CSP). This invention is simpler than the previous prior art and the advantages of the invention are the back side photoresist and the trench filled with the filling material can be easily tested before the cutting process is conducted. And after the cutting process, it

is easily cut along the trench to separate each chip on the wafer 2, as shown in FIG.13.

The wafer level package of this invention is shown in FIG.11, which possesses a plurality of chips on the wafer 2. The trenches 20 are formed therein to run through the wafer 2. The filling material 22 is filled in the trench 20. Metal pads 4 are formed on the surface of the wafer 2. The photosensitive polymer 8, such as photosensitive polyimide or epoxy is formed on the surface of the wafer 2 and exposed the metal pads 4, the first conductive layer 12 lies within the photosensitive polymer 8, the metal wire 18 lies above the surface of the filling material 22 and the first conductive layer 12. A protection layer is covered on the top of the metal wire 18, and the photosensitive polymer 8 and it also exposes a portion of the metal wire 18 and the conductive bump 24, which is on the top of the exposed metal wire 18.

As will be understood by persons skilled in the art, the foregoing preferred embodiment of the present invention is illustrative of the present invention rather than limiting the present invention. Having described the invention in connection with a preferred embodiment, modification will now suggest itself to those skilled in the art. Thus, the invention is not to be limited to this embodiment, but rather the invention is intended to cover various modifications and similar arrangements included within the spirit and scope of the appended claims, the scope of which should be accorded the broadest interpretation so as to encompass all such modification and similar structure.

While the preferred embodiment of the invention has been illustrated and described, it will be appreciated that various changes can be made therein without departing from the spirit and scope of the invention.